

REMARKS

This Amendment is filed in response to the Office Action dated January 3, 2005, which has a shortened statutory period set to expire April 3, 2005.

Claims 1-23 Are Patentable Over The Cited References

Claims 1 and 12, as amended, now recite:

a modified Brokaw cell including a first transistor and a second transistor, each transistor including:

a bipolar transistor having a base, an emitter, and a lateral collector; and

a parasitic transistor having a source coupled to the emitter of the bipolar transistor, a drain coupled to the lateral collector of the bipolar transistor, and a substrate coupled to the base of the bipolar transistor.

Applicant respectfully submits that none of the cited references teach these limitations. Because O'Neill, Dooley, Gilbert, Gramegna, and Fujimori, either individually or in combination, fail to disclose or suggest these limitations, Applicant requests reconsideration and withdrawal of the rejections of Claims 1 and 12.

Claims 4-11 depend from Claim 1 and therefore are patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 4-11.

Claims 14-21 depend from Claim 12 and therefore are patentable for at least the reasons presented for Claim 12. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 14-21.

Moreover, Claim 2, as amended, now recites:

a modified Brokaw cell including a first transistor and a second transistor, each

transistor including a base, an emitter, and a collector; and

a cascode amplifier, wherein collectors of the first and second transistors in the modified Brokaw cell are folded into input terminals of the cascode amplifier,

wherein an output of the bandgap reference voltage circuit provides a source voltage to the cascode amplifier.

Similarly, Claim 13, as amended, now recites:

a modified Brokaw cell including a first transistor and a second transistor, each transistor including a base, an emitter, and a collector; and

a cascode amplifier, wherein collectors of the first and second transistors in the modified Brokaw cell are folded into input terminals of the cascode amplifier,

wherein an output of the shunt regulator provides a source voltage to the cascode amplifier.

As taught by Applicant in the Specification:

[0012] Brokaw cell 200 (Figure 2) can be implemented in CMOS technology. Unfortunately, operational amplifier 207 derives its source voltage from the input voltage V_{IN} . In this configuration, i.e. with its control terminal coupled to V_{IN} , any variation in input voltage can also affect amplifier 207, thereby adversely affecting the stability of the bandgap reference voltage V_Z . Specifically, even a few millivolts of offset introduced in operational amplifier 207 can result in an inability to accurately detect the voltage differential between its positive and negative input terminals. This detection problem, called power supply rejection (PSR), can render Brokaw cell 200 inapplicable for any system in which the input voltage may vary. Unfortunately, most systems have some variation in input voltage, either intentionally or unintentionally.

[0013] Therefore, a need arises for a bandgap reference voltage circuit that can be manufactured in CMOS technology while preserving the accuracy of the bandgap reference voltage irrespective of input voltage variations.

Therefore, the recited configurations of Claims 2 and 13 provide distinct advantages. Specifically, as taught by Applicant in the Specification:

[0015] Of importance, the source voltage to the cascode amplifier can be advantageously tied to the output of the bandgap reference voltage circuit. That is, the cascode amplifier can operate using the bandgap reference voltage (i.e. 1.2 V). By using this source voltage, which is ensured to be stable, the cascode amplifier will remain unaffected by any variation in the input voltage.

Applicant respectfully submits that the cited references fail to disclose or suggest the limitations recited in Claims 2 and 13.

Specifically, the Office Action characterizes transistors 202, 204, 206, and 208 of O'Neill as being the recited first and second transistors. However, O'Neill fails to teach that the collectors of the first and second transistors are folded into input terminals of the cascode amplifier. O'Neill also fails to teach that an output of the bandgap reference voltage circuit (or the shunt regulator) provides a source voltage to the cascode amplifier.

Dooley fails to remedy the deficiency of O'Neill with respect to Claims 2 and 13. The Office Action fails to indicate any particular elements or passages to the contrary.

Gilbert fails to remedy the deficiency of O'Neill and Dooley with respect to Claims 2 and 13. The Office Action cites col. 8, lines 25-45 as teaching a modified Brokaw cell. However, this passage teaches nothing regarding the recited limitations of Claims 2 and 13.

Gramegna fails to remedy the deficiency of O'Neill, Dooley, and Gilbert with respect to Claims 2 and 13. The Office Action cites the Abstract, lines 10-15 as teaching an output shunt

regulator. However, this passage teaches nothing regarding the recited limitations of Claims 2 and 13.

Fujimori fails to remedy the deficiency of O'Neill, Dooley, Gilbert, and Gramegna with respect to Claims 2 and 13. The Office Action cites figure 9 as teaching NMOS and PMOS transistor configurations. However, this figure teaches nothing regarding the recited limitations of Claims 2 and 13.

Because the cited references, either individually or in combination, fail to disclose or suggest the limitations recited in Claims 2 and 13, Applicant requests reconsideration and withdrawal of the rejection of Claims 2 and 13.

Claim 3 depends from Claim 2 and therefore is patentable for at least the reasons presented for Claim 2. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 3.

Claim 22, which is amended to correct a minor informality, recites a cascode amplifier comprising:

- a bias current circuit connected to a regulated voltage source;
- a first NMOS transistor;
- a second NMOS transistor;
- a third NMOS transistor; and
- a fourth NMOS transistor,

wherein a drain of the first NMOS transistor is connected to a source of the third NMOS transistor and to a first input terminal of the cascode amplifier, a drain of the second NMOS transistor is connected to a source of the fourth NMOS transistor and a second input terminal of the cascode amplifier, and sources of the first and second NMOS transistors are connected to a low voltage source VSS,

wherein substrates of the first, second, third, and fourth NMOS transistors are connected to VSS,

wherein gates of the first, second, third, and fourth NMOS transistors and a drain of the third NMOS transistor are connected to a common

node, which is connected to a bias current source, and

wherein a drain of the fourth NMOS transistor is connected to an output terminal of the cascode amplifier.

Applicant respectfully submits that the cited references fail to teach this configuration. The Office Action cites figure 9 of Fujimori as teaching NMOS and PMOS transistor configurations. However, this figure teaches nothing regarding the recited limitations of Claims 22. The other cited references, i.e. O'Neill, Dooley, Gilbert, and Gramegna, fail to remedy the deficiency of Fujimori with respect to Claim 22.

Because the cited references, either individually or in combination, fail to disclose or suggest the limitations recited in Claim 22, Applicant requests reconsideration and withdrawal of the rejection of Claim 22.

Claim 23 depends from Claim 22 and therefore is patentable for at least the reasons presented for Claim 22. Based on these reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 23.

CONCLUSION

Claims 1-23 are pending in the present Application.
Allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 15, 2005.

4/15/2005
Date

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